ABSTRACT OF THE DISCLOSURE

A decoder and a decoding method can perform log-sum corrections by means of linear approximation, putting stress on speed, with a reduced circuit dimension without adversely affecting the decoding performance of the circuit. The decoder comprises a linear approximation circuit 68 added to obtain log likelihoods and adapted to compute the correction term expressed in a one-dimensional function of a variable by linear approximation. The linear approximation circuit 68 computes the correction term by log-sum corrections by means of linear approximation using function $F = -a\,|P - Q| + b$, where the coefficient -a representing the gradient of the function and the coefficient b representing the intercept are expressed by a power exponent of 2. More specifically, when the coefficients a and b are expressed respectively by -2^{-k} and $2^m - 1$, the linear approximation circuit 68 discards from the lowest bit the k-th lowest bits, bit-shifts the absolute value data $|P - Q|$ and then inverts the m bits from the k+1-th lowest bit to the m+k-th lowest bit by means of inverter 91.